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(54) Electronic device having pseudo-SRAM.

(57) An electronic device uses a pseudo-SRAM (14) having a self-refreshing function, as a memory, and a refresh timing signal having a predetermined period is supplied to the pseudo-SRAM in the operation state of the electronic device. When no key operation is performed with a keyboard (17) for a predetermined period of time, the electronic device switches a mode into an idle mode to stop supply of an operation clock to a CPU (11) and to stop supply of the timing signal to the pseudo-SRAM. When the supply of the timing signal to the pseudo-SRAM is stopped, the pseudo-SRAM operates the self-refreshing function for holding data with low power consumption. When a key operation is detected in the idle mode, a refresh timing signal having a high frequency is supplied to the pseudo-SRAM for a predetermined period of time. Thereafter, the supply of a clock to the CPU is restarted, and the state of the electronic device is returned to a normal operation state.

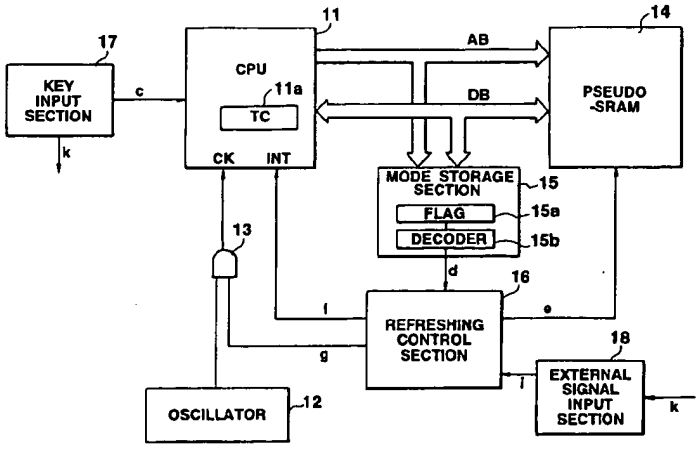

FIG.1

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The present invention relates to an electronic device such as an electronic notebook or a compact electronic calculator which is driven by a battery power supply and uses a pseudo-SRAM, having a self-refreshing function, as a data memory.

In a conventional electronic device such as an electronic notebook or a compact electronic calculator driven by a battery power supply, when a DRAM which must be refreshed is used as a memory, refresh pulses must be supplied to the DRAM at a predetermined interval. In addition, even in a device using a pseudo-SRAM having a self-refreshing function, although the self-refreshing function is used in a power-off state, the self-refreshing function is not used in a power-on state because timing control is complicated in a normal operation state. Therefore, in the normal operation state or use of the device, refresh pulses are always supplied to the DRAM or the pseudo-SRAM at a predetermined interval.

However, in such an electronic device using a battery power supply, as in a case wherein a key input operation or communication is not performed for a long period of time in a normal operation state, even when a CPU is not actually operated, clocks and refresh pulses are kept supplied to the CPU and a memory. For this reason, the power of the battery power supply is wasted.

The present invention has been made in consideration of the above circumstances, and has as its object to provide an electronic device capable of preventing power consumption from being wasted in a state in which a CPU waits for a key input operation for a long period of time even when the power supply of the electronic device is set in an ON state.

More specifically, according to one aspect of the present invention, there is provided an electronic device an electronic device comprising: a CPU for controlling an operation of the electronic device; a pseudo-SRAM having a self-refreshing function; storage means for storing operation modes of the electronic device; and control means for controlling an operation clock supplied to the CPU in accordance with the operation modes stored in the storage means and controlling a refresh timing signal supplied to the pseudo-SRAM.

According to another aspect of the invention, there is provided an electronic device an electronic device comprising: key input unit; a CPU for performing a process corresponding to a key operation of the key input unit; a pseudo-SRAM having a self-refreshing function; and refresh timing signal control means for supplying a first refresh timing signal having a predetermined period to the pseudo-SRAM in an operation state of the CPU, and stopping supply of the first refresh timing signal when no key operation is performed with the key input unit for a predetermined period of time.

This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

FIG. 1 is a block diagram showing a circuit arrangement according to an embodiment of the present invention;

FIG. 2 is a block diagram showing the detailed circuit arrangement in the refreshing control section in FIG. 1;

FIG. 3 is a flow chart showing the operation of this embodiment device when an active mode is switched to an idle mode; and

FIG. 4 shows a timing chart for explaining an operation according to this embodiment.

FIG. 1 shows the basic circuit arrangement of the main part of an electronic device according to an embodiment of the present invention. Reference numeral 11 denotes a CPU for performing a control operation of the entire device. This CPU 11 is operated such that an operation clock generated by an oscillator 12 is input to the CPU 11 through an AND circuit 13. The CPU 11 is connected to a pseudo-SRAM 14 for storing various data and a mode storage section 15 through an address bus AB and a data bus DB. The CPU 11 receives a key signal C from a key input section 17 to perform a process corresponding to a key operation.

The mode storage section 15 stores information corresponding to three modes (to be described later) of the electronic device in a flag memory 15a. The mode information is decoded by a decoder 15b. When an idle mode is set, a signal d is output to a refreshing control section 16.

The refreshing control section 16 controls the pseudo-SRAM 14 and the CPU 11 in accordance with a set mode and outputs an interrupt signal f, a gate control signal g, and a refresh timing pulse e corresponding to a mode state to the CPU 11, the AND circuit 13, and the pseudo-SRAM 14, respectively. On the other hand, the refreshing control section 16 receives a start signal i from an external signal input section 18.

This external signal input section 18 sends the start signal i to the refreshing control section 16 in response to an input of a signal k representing that a key operation is performed with the key input section 17.

The detailed circuit arrangement in the refreshing control section 16 will be described below with reference to FIG. 2. Referring to FIG. 2, the idle mode signal d from the mode storage section 15 and the start signal i from the external signal input section 18 are input to a control circuit 21. A carry signal from a sexidecimal counter 25 is input to the control circuit 21. The control circuit 21 generates

the interrupt signal f and the gate control signal g on the basis of the mode signal d the start signal i, and the carry signal, outputs the interrupt signal f and the gate control signal g to the CPU 11 and the AND circuit 13, respectively, and sends a switching/selecting signal to a switching circuit 22.

A timing signal which is sent from a first timing signal circuit 23 for automatically refreshing the pseudo-SRAM 14 or a timing signal which is sent from a second timing signal circuit 24 for refreshing the pseudo-SRAM 14 at a time is selected by the switching circuit 22 in accordance with the selecting signal from the control circuit 21. The selected timing signal is supplied to the pseudo-SRAM 14 and the sexidecimal counter 25 as a refresh timing pulse e.

The sexidecimal counter 25 is reset by the control circuit 21 to count refresh timing pulses e sent through the switching circuit 22. When the count value of the sexidecimal counter 25 becomes 16, the sexidecimal counter 25 sends a carry signal to the control circuit 21.

The operation of the embodiment described above will be described below.

In this device, three modes, i.e., an "active mode" in which the CPU 11 and other circuits are fully operated, an "idle mode" in which a key input waiting state is set to reduce the power consumption of a battery, and a "standby mode" in which a completely suspended state is set by turning off the battery of the electronic device, are set.

In the "active mode", the CPU 11 and the pseudo-SRAM 14 are always operated to perform a process corresponding to a key input operation. The refreshing control section 16 supplies a refresh timing pulse e having a predetermined period to the pseudo-SRAM 14. The pseudo-SRAM 14 backs up its storage contents using an automatic refreshing function which is a conventional technique. At this time, the gate control signal g goes to "H" level, and the gate of the AND circuit 13 is set in an open state. For this reason, an operation clock generated by the oscillator 12 is continuously supplied to the CPU 11 through the AND circuit 13.

In the "idle mode", a gate control signal g output from the refreshing control section 16 goes to "L" level, and the gate of the AND circuit 13 is set in a closed state. For this reason, the operation clock generated by the oscillator 12 is not supplied to the CPU 11, and the CPU 11 is set in a disabled state. At this time, the output of the refresh timing pulse e from the refreshing control section 16 to the pseudo-SRAM 14 is disabled. When the pseudo-SRAM 14 detects the absence of the refresh timing pulse e in a predetermined period of time, the pseudo-SRAM 14 performs a self-refreshing function to back up the storage contents of the pseudo-SRAM 14.

In the "standby mode", since power supply to the circuits except for the pseudo-SRAM 14 is stopped, the pseudo-SRAM 14 performs the self-refreshing function to back up the storage contents of the pseudo-SRAM 14.

An operation for shifting the "active mode" to the "idle mode" and then the "idle mode" to the "active mode" while the power supply of the electronic device is set in an ON state will be described below with reference to FIGS. 3 and 4.

When a key input operation is performed in the "active mode", a time counter 11a in the CPU 11 is reset and the CPU 11 performs a process corresponding to the key operation (steps S1 to S3).

In the "active mode", when a state in which any key input operation is not performed is continued, the count value of the time counter 11a is incremented (steps S1, S4, and S5). When a predetermined period of time, e.g., 5 minutes, has passed, the count-over state of the time counter 11a is detected (step S4), set mode information representing, e.g., "00", the "active mode" stored in the flag memory 15a of the mode storage section 15 is rewritten with set mode information, e.g., "01", representing the "idle mode" (S6).

When the "idle mode" is set, the refreshing control section 16 immediately causes the gate control signal g to the AND circuit 13 to go from "H" level to "L" level in response to the output d from the decoder 15b. Therefore, as shown in (5) in FIG. 4, supply of an operation clock generated by the oscillator 12 to the CPU 11 is interrupted. Subsequently, a timing signal which is for an automatic refreshing function, is output from the first timing signal circuit 23, and has been selected up to this is interrupted, and as shown in (2) in FIG. 4, supply of the refresh timing pulse e to the pseudo-SRAM 14 is disabled.

The characteristics of the pseudo-SRAM 14 will be described below. It is assumed that the pseudo-SRAM 14 must be refreshed at a period of 2048 pulses/32 [ms]. Therefore, the first timing signal circuit 23 generates a first timing signal having a period of one pulse/15 [μs] obtained by averaging the period of 2048 pulses/32 [ms] to use the first timing signal for an automatic refreshing operation, and the first timing signal circuit 23 supplies the generated timing signal to the pseudo-SRAM 14 in the "active mode". In this state, the current consumption value of the pseudo-SRAM 14 is, e.g., about 300 [μA].

However, in the pseudo-SRAM 14, when a predetermined period of time has passed from when the refresh timing pulse e is disabled, the self-refreshing function is started, and the storage contents are backed up by an internal circuit (not shown) of the pseudo-SRAM 14 with minimum current consumption.

In the "idle mode", since no operation clock is supplied to the CPU 11, the power consumption of the CPU 11 becomes "0". In addition, since the pseudo-SRAM 14 consumes only a minimum current, e.g., a current of about 30 [μA], required to back up the storage contents of the pseudo-SRAM 14 using the self-refreshing function, the power consumption of the entire circuit can be considerably reduced.

When a key input operation is performed, the signal k representing that a key input operation is performed is input to the external signal input section 18. The external signal input section 18 which receives the signal k causes the start signal i to the refreshing control section 16 to go to "H" level as shown in (3) in FIG. 4.

In response to the start signal i, the control circuit 21 of the refreshing control section 16 causes the switching circuit 22 to select a second timing signal output from the second timing signal circuit 24 for a refreshing-at-a-time operation, and supplies the second timing signal to the pseudo-SRAM 14 and the sexidecimal counter 25 as shown in (2) in FIG. 4.

The second timing signal output from the second timing signal circuit 24 for the refreshing-at-a-time operation has a period of, e.g., about 16 pulses/10 [μs]. It is assumed that the second timing signal is a timing signal having a frequency considerably higher than that of the first timing signal used for the automatic refreshing operation.

When 16 second timing signals output from the second timing signal circuit 24 are supplied to the pseudo-SRAM 14 as the refresh timing pulses e for 10 [μs], a refreshing operation is not required for 230 [μs] after the 16 second signals are supplied, as indicated by a calculation of "15 [μs] x 16 - 10 [μs] = 230 [μs]".

The sexidecimal counter 25 counts second timing signals output from the second timing signal circuit 24 after the sexidecimal counter 25 is reset by the reset signal R of the control circuit 21, and sends a carry signal to the control circuit 21 when the count value of the sexidecimal counter 25 is set to be "16".

In response to the carry signal from the sexidecimal counter 25, the control circuit 21 causes the gate control signal g which is to be supplied to the AND circuit 13 and has been set at "L" level to go to "H" level, so as to restart supply of an operation clock generated by the oscillator 12 to the CPU 11 as shown in (5) in FIG. 4. At the same time, as shown in (4) in FIG. 4, the control circuit 21 sends a pulse serving as an interrupt signal f to the CPU 11 to perform a starting process in a restart state.

However, in the CPU 11, the starting process in the restart state is performed in accordance with the interrupt signal f (step S7 of FIG. 3). At this time, since the pseudo-SRAM 14 need not be refreshed for 230 [μs] because the refreshing-at-a-time operation is performed, the CPU 11 can involve in the starting process with a time margin. The CPU 11 performs the starting process and rewrites set mode information, e.g., "01", representing the "idle mode" and stores in the mode storage section 15 with set mode information, e.g., "00", representing the "active mode", thereby returning to the "active mode" again.

Subsequently, upon completion of the starting process of the CPU 11, before the period of time (230 [μs]) which requires no refreshing operation has passed, the control circuit 21 causes the switching circuit 22 to select the first timing signal output from the first timing signal circuit 23 for an automatic refreshing operation, and the control circuit 21 supplies the first timing signal to the pseudo-SRAM 14.

Although the "standby mode" is a mode in which the power supply is turned off to perform the self-refreshing function of the pseudo-SRAM 14, a description of the self-refreshing function will be omitted because the self-refreshing function of the pseudo-SRAM is known well.

As has been described above, according to the present invention, when the CPU waits for a key input operation for a long period of time in the operation state of the electronic device, the "idle mode" is set, power is prevented from being wasted. Thereafter, when a key input operation is performed, the state of the electronic device including the contents of the memory can be rapidly returned to the operation state set before the CPU waits for the key input operation.

Claims

1. An electronic device comprising:
   a CPU (11) for controlling an operation of said electronic device;
   a pseudo-SRAM (14) having a self-refreshing function;
   storage means (15) for storing operation modes of said electronic device; and
   control means (16) for controlling an operation clock supplied to said CPU in accordance with the operation modes stored in said storage means and controlling a refresh timing signal supplied to said pseudo-SRAM.

2. A device according to claim 1, characterized in that said storage means (15) for storing the operation modes has means (15a) for storing at least an active mode and an idle mode, the active mode being a mode in which said CPU is operated, and the idle mode being a mode

in which said CPU is not operated.

3. A device according to claim 2, characterized in that said control means (16) has means (21, 22, 23) for supplying a first refresh timing signal having a predetermined period to said pseudo-SRAM in the active mode to cause said pseudo-SRAM to perform an automatic refreshing operation, and stopping supply of the first refresh timing signal in the idle mode.

4. A device according to claim 3, characterized in that said control means has means (13) for stopping supply of an operation clock to said CPU in the idle mode.

5. A device according to claim 4, characterized by further comprising key input means (17) for performing key operation, detection means (11a) for detecting that no key input operation is performed with said key input means for a predetermined period of time, and means (11, 15a) for switching a mode from the active mode to the idle mode when said detection means detects that no key input operation is performed for the predetermined period of time.

6. A device according to claim 5, characterized by further comprising detection means (18) for detecting that a key input operation is performed in the idle mode, and means (16, 11) for switching a mode from the idle mode to the active mode when said detection means detects that the key input operation is performed in the idle mode.

7. A device according to claim 6, characterized in that said control means has supply means (21, 22, 24) for supplying a second refresh timing signal having a period shorter than that of the first refresh timing signal to said pseudo-SRAM for a predetermined period of time when a mode is switched from the idle mode to the active mode.

8. A device according to claim 7, characterized by further comprising first signal generation means (23) for generating the first refresh timing signal, and second signal generation means (24) for generating the second refresh timing signal.

9. A device according to claim 8, characterized in that said supply means has a counter (25) for counting generation pulses of the second refresh timing signal by a predetermined number.

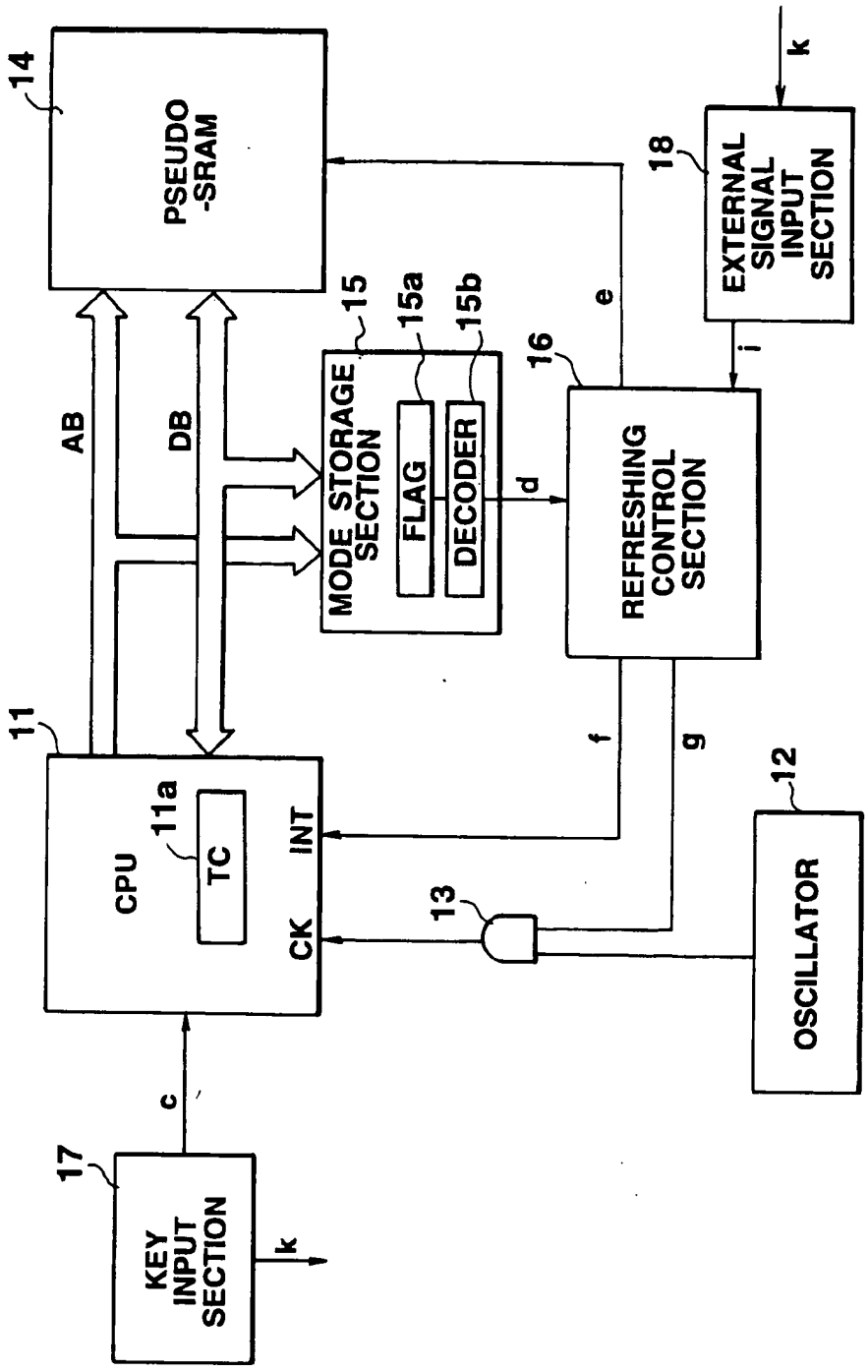

14
PSEUDO -SRAM
18
EXTERNAL SIGNAL INPUT SECTION
k
AB
DB
15
15a
15b
MODE STORAGE SECTION
FLAG
DECODER
e
16
REFRESHING CONTROL SECTION
i
d
11
CPU
11a
TC
INT
CK
f
g
12
OSCILLATOR
13
c
17
KEY INPUT SECTION
k

FIG.1

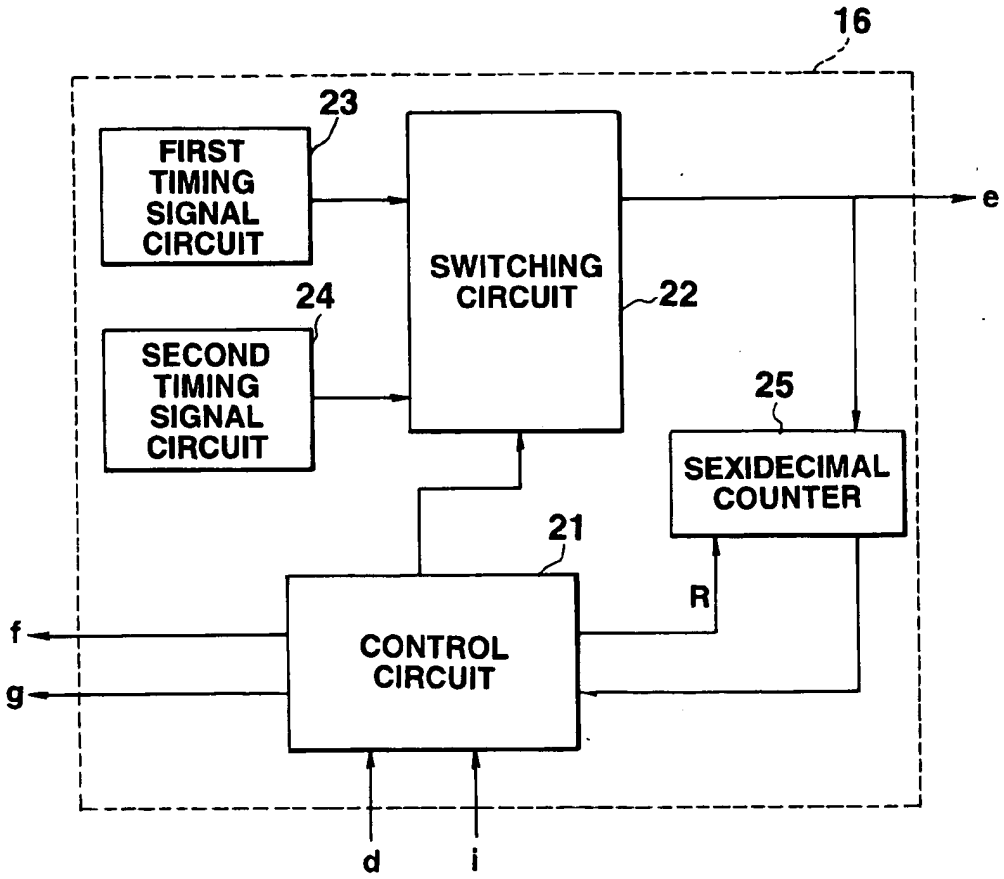

16
23
FIRST TIMING SIGNAL CIRCUIT
24
SECOND TIMING SIGNAL CIRCUIT
SWITCHING CIRCUIT
22
e
25
SEXIDECIMAL COUNTER
21
R
CONTROL CIRCUIT
f
g
d
i

FIG.2

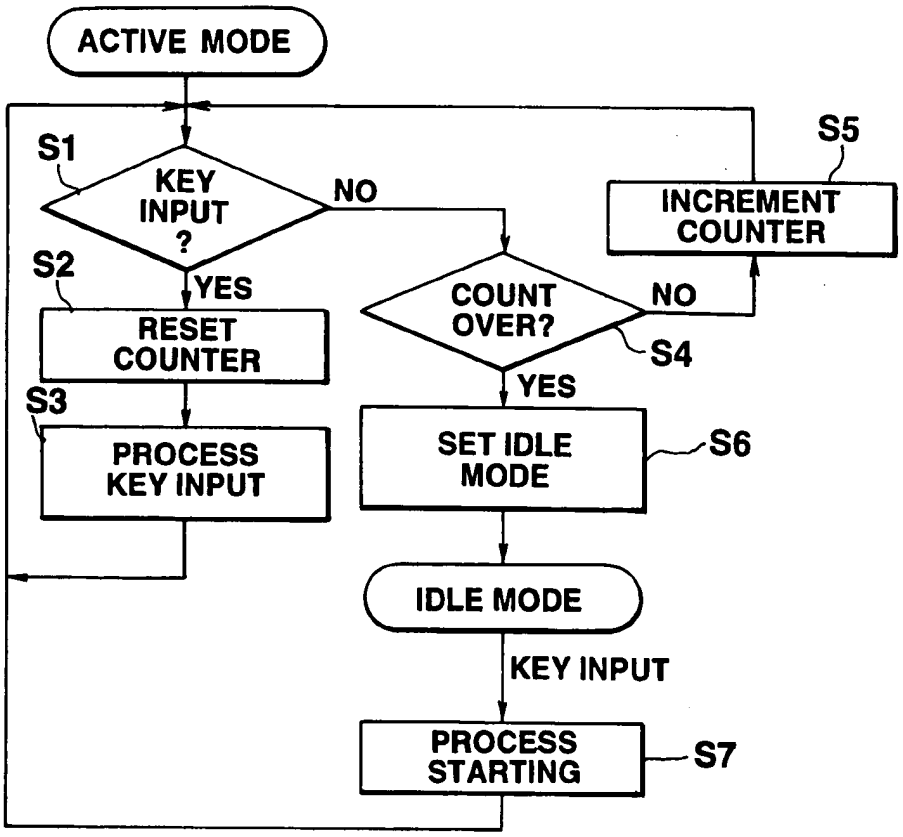
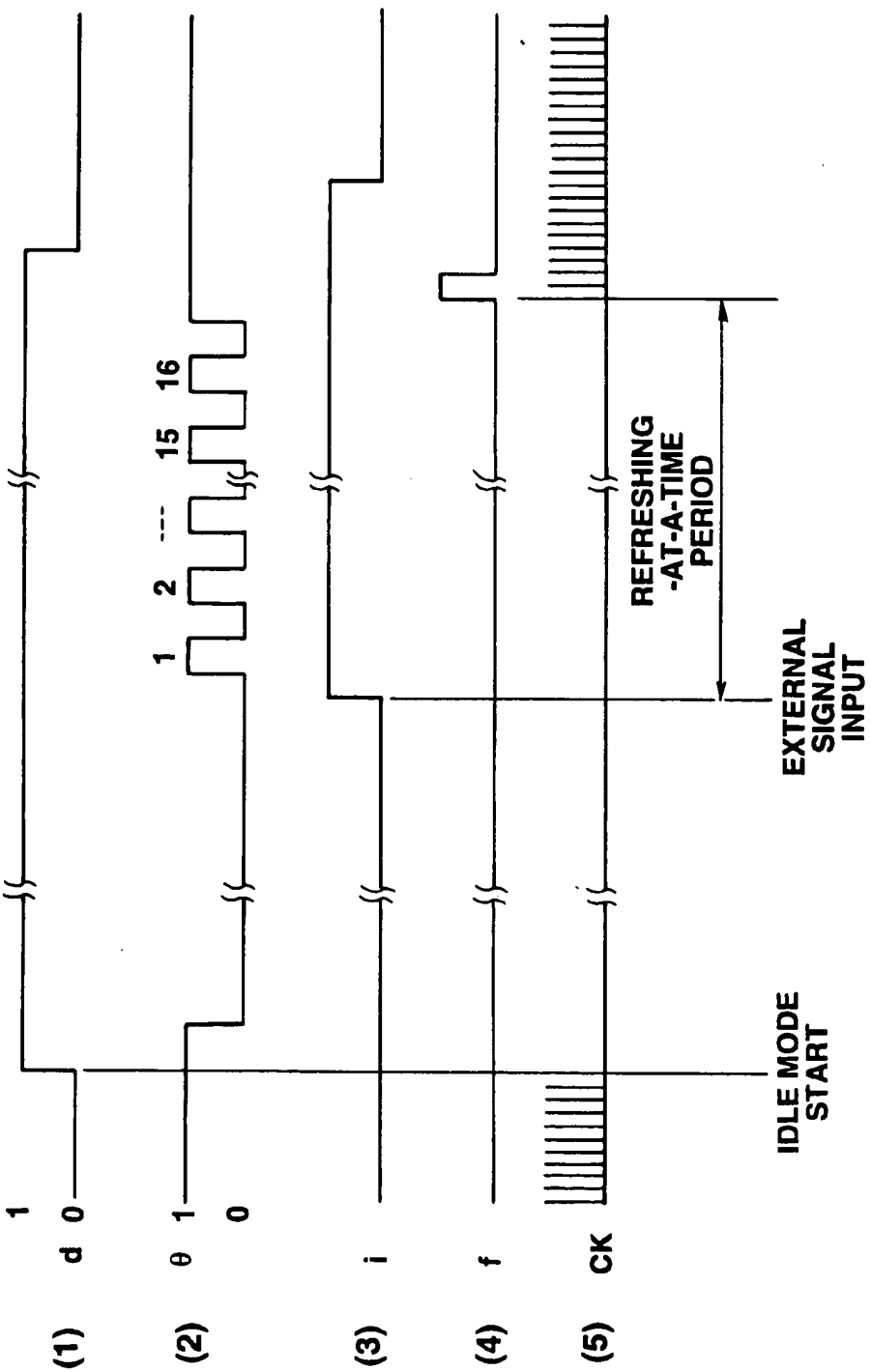

ACTIVE MODE
S1
KEY INPUT ?
NO
YES
S2
RESET COUNTER
S3
PROCESS KEY INPUT
COUNT OVER?
NO
S4
YES
S5
INCREMENT COUNTER
SET IDLE MODE
S6
IDLE MODE
KEY INPUT
PROCESS STARTING
S7

FIG.3


(1)
d
1
0
(2)
θ
1
0
1
2

15
16
(3)
i
(4)
f
(5)
CK
IDLE MODE START
REFRESHING -AT-A-TIME PERIOD
EXTERNAL SIGNAL INPUT

FIG.4